In the Claims:

The following are pending in this application and the status of each is listed below. This listing supercedes and replaces all prior listings.

1. (Original) A signal processor, comprising:

a pulse width modulator having a clock rate; and

a digital filter configured to receive an output of said pulse width modulator, wherein said output comprises a distortion, and wherein said digital filter samples said output at said clock rate to suppress said distortion.

2. (Currently amended) The signal processor of claim 1, further comprising an oversampling modulator upstream of and coupled to said pulse width modulator.

3. (Original) The signal processor of claim 2, wherein said oversampling modulator comprises a sigma-delta type modulator.

4. (Cancelled)

5. (Currently amended) The signal processor of claim [[4]] 3, wherein said oversampling modulator generates an oversampled signal having a period and a total number of levels, and wherein said clock rate is at least M times said period, where M is said total number of levels in said oversampled signal.

6. (Original) The signal processor of claim 5, wherein said sigma-delta type modulator comprises a first order sigma-delta type modulator.

7. (Previously presented) The signal processor of claim 3, further comprising a filter upstream of said pulse width modulator.

8. (Original) The signal processor of claim 1, wherein said digital filter comprises an IIR filter.

9. (Original) The signal processor of claim 8, wherein said IIR filter comprises a single pole filter.

10. (Original) The signal processor of claim 1, wherein said digital filter comprises a low pass filter.

11. (Original) The signal processor of claim 1, further comprising a feedback path comprising said digital filter.

12. (Original) An integrated circuit chip system comprising the signal processor of claim 1.

13. (Original) The integrated circuit chip system of claim 12, wherein said system provides a two-channel output.

14. (Original) The integrated circuit chip system of claim 12, wherein said system provides an eight-channel output.

15. (Original) A portable audio player comprising the signal processor of claim 1.

16. (Original) The portable audio player of claim 15, further comprising a digital audio signal source.

17. (Currently amended) The portable audio player of claim [[10]] 15, wherein said digital audio source comprises a memory medium reader.

18. (Original) The portable audio player of claim 17, wherein said memory medium reader comprises an optical disk reader.

19. (Original) The portable audio player of claim 16, wherein said digital audio signal source comprises a memory for storage of a digital audio file.

20. (Original) The portable audio player of claim 16, wherein said digital audio signal source comprises a digital receiver.

21. (Original) An audio power amplification system comprising the signal processor of claim 1.

22. (Previously presented) The audio power amplification system of claim 21, further comprising an RC type demodulation filter.

23. (Original) A digital circuit for suppressing a distortion in a digital signal that exists after a pulse width modulation, wherein said pulse width modulation occurs at a clock rate, and wherein said digital circuit comprises a digital filter configured to receive said signal having said distortion and to sample said signal at said clock rate to suppress said distortion.

24. (Original) A digital signal processing circuit, comprising:

a pulse width modulator having an output with a distortion; and

means for sampling said output and suppressing said distortion in a digital domain.

25. (Original) The digital signal processing circuit of claim 24, further comprising an oversampling modulator.

26. (Original) The digital signal processing circuit of claim 25, wherein said oversampling modulator comprises a sigma-delta type modulator.

27. (Original) The digital signal processing circuit of claim 26, wherein said sigma-delta type modulator comprises a first order sigma-delta type modulator.

28. (Original) The digital signal processing circuit of claim 25, wherein said oversampling modulator is upstream of said pulse width modulator.

29. (Previoulsy presented) The digital signal processing circuit of claim 28, wherein said oversampling modulator generates an oversampled signal having a period and a total number of levels, and said pulse width modulator operates at a clock rate that is at least M times said period, where M is said total number of levels in said oversampled signal.

30. (Previously presented) The digital signal processing circuit of claim 25, further comprising a filter upstream of said pulse width modulator.

31. (Original) An integrated circuit chip system comprising the signal processor of claim 24.

32. (Original) The integrated circuit chip system of claim 31, wherein said system provides a two-channel output.

33. (Original) The integrated circuit chip system of claim 31, wherein said system provides an eight-channel output.

34. (Original) An audio power amplification system comprising the signal processor of claim 24.

35. (Original) The audio power amplification system of claim 34, further comprising an RC type demodulation filter.

36. (Original) A portable audio player comprising the signal processor of claim 24.

37. (Original) The portable audio player of claim 36, further comprising a digital audio signal source.

38. (Original) The portable audio player of claim 37, wherein said digital audio signal source comprises a memory medium reader.

39. (Original) The portable audio player of claim 38, wherein said memory medium reader comprises an optical disk reader.

40. (Original) The portable audio player of claim 37, wherein said digital audio signal source comprises a memory for storage of a digital audio file.

41. (Original) The portable audio player of claim 37, wherein said digital audio signal source comprises a digital receiver.

42. (Original) The digital signal processing circuit of claim 24, wherein said sampling occurs at a clock rate of said pulse width modulator.

43. (Previously presented) A signal processor for modulating a digital input signal, comprising a closed loop digital circuit comprising:

a forward path comprising a first filter stage coupled with and upstream from an encoder stage, wherein said encoder stage comprises a first order sigma-delta type modulator and a pulse width modulator, wherein said sigma-delta type modulator generates an oversampled signal having a period and a total number of levels, and said pulse width modulator operates at a clock rate that is at least M times said period, where M is said total number of levels in said oversampled signal, and wherein said forward path produces an output having a distortion; and

a feedback path comprising a digital filter that samples said output in a digital domain to suppress said distortion.

44. (Original) The signal processor of claim 43, wherein said digital filter samples said output at said clock rate.

45. (Original) The signal processor of claim 43, wherein said signal processor exhibits a modulation depth of up to about –1 db in an audio frequency band.

46. (Original) The signal processor of claim 43, wherein said signal processor reduces a total harmonic distortion to about 90 – 100 db.

47. (Cancelled)

48. (Previously presented) An integrated circuit chip configured to receive a pulse code modulated digital signal and to generate a pulse width modulated digital output signal, wherein said output signal has a distortion, and wherein said distortion is

suppressed by a digital filter that operates at at least a clock rate of said pulse width modulated digital signal.

49. (Original) A method, comprising:

modulating a first pulse code modulated signal having a first resolution into a second pulse code modulated signal having a second resolution, wherein said second resolution is smaller than said first resolution;

modulating said second pulse code modulated signal into a third signal comprising a plurality of pulses in time having a clock rate; and

filtering in a digital domain said plurality of pulses in time to suppress a distortion in said third signal.

50. (Original) The method of claim 49, wherein said first resolution is between 12 bits and 24 bits inclusively.

51. (Original) The method of claim 50, wherein said first resolution is 16 bits.

52. (Original) The method of claim 50, wherein said second resolution is between 2 bits and 6 bits inclusively.

53. (Original) The method of claim 52, wherein said second resolution is 4 bits.

54. (Original) The method of claim 49, wherein said modulating said first pulse code modulated signal comprises using a sigma-delta type modulator.

55. (Original) The method of claim 54, wherein said sigma-delta type modulator is a first order sigma-delta type modulator.

56. (Original) The method of claim 49, wherein said modulating said second pulse code modulated signal comprises using a pulse width modulator.

57. (Original) The method of claim 49, wherein said filtering comprises using

a digital filter.

58. (Original) The method of claim 57, wherein said digital filter comprises an IIR filter.

59. (Original) The method of claim 58, wherein said IIR filter comprises a single pole filter.

60. (Original) The method of claim 57, wherein said digital filter comprises a low pass filter.

61. (Original) The method of claim 49, wherein said filtering comprises forming a feedback signal having said first resolution.

62. (Original) The method of claim 49, wherein said plurality of pulses in time is a substantially small range of pulses in time.

63. (Previously presented) The method of claim 49, wherein said modulating said first pulse code modulated signal comprises generating an oversampled signal having a period and a total number of levels, wherein said modulating said second pulse code modulated digital signal occurs at a clock rate that is at least M times said period, where M is said total number of levels in said oversampled signal.

64. (Original) The method of claim 49, wherein said filtering comprises sampling at said clock rate.

65. (Original) The method of claim 49, further comprising amplifying said third signal to produce an amplified output.

66. (Original) The method of claim 65, further comprising creating an analog signal from said amplified output.

67. (Original) The method of claim 66, wherein said creating comprises using an RC filter circuit.

68. (Original) A device, comprising:

means for modulating a first pulse code modulated signal having a first resolution into a second pulse code modulated signal having a second resolution, wherein said second resolution is smaller than said first resolution;

means for modulating said second pulse code modulated signal into a third signal comprising a plurality of pulses in time having a clock rate; and

means for filtering in a digital domain said plurality of pulses in time to suppress a distortion in said third signal.

69. (Previously presented) The signal processor of claim 7, wherein the filter is an integrator.

70. (Previously presented) The digital signal processing circuit of claim 30, wherein the filter is an integrator.

71. (Previously presented) The signal processor of claim 43, wherein said signal processor exhibits a modulation depth of up to about 0 db in an audio frequency band.

72. (Previously presented) The signal processor of claim 43, wherein said signal processor reduces a total harmonic distortion to about 90 – 140 db.

73. (Previously presented) The method of claim 49, wherein said first resolution is between 12 bits and 24 bits inclusively.

74. (New) A loop that corrects distortion caused by transforming an oversampled pulse code modulated signal to a pulse width modulated signal, including;

a wide-bit input signal;

a summing element accepting the wide-bit input signal;

an input filter coupled to the difference element;

an oversampler coupled to the input filter, producing an oversampled signal having less precision and higher frequency than the wide-bit signal;

a pulse width modulator coupled to the oversampler;

an output coupled to the pulse width modulator; and

a digital feedback filter coupled to the pulse width modulator, the digital feedback filter

producing a correction signal that at least partially compensates for undesired distortion introduced by the pulse width modulator,

formating the correction signal to match precision and frequency of the wide-bit input signal and

feeding back the formatted correction signal to the summing element.

75. (New) The loop of claim 74, wherein the summing element calculates a difference between the wide-bit input signal and the formatted correction signal.

76. (New) The loop of claim 74, wherein input filter is an integrator.

77. (New) The loop of claim 74, wherein input filter is a second order element of the oversampler.

78. (New) The loop of claim 74, wherein the digital feedback filter is a single pole IIR filter.

79. (New) The loop of claim 74, wherein the digital feedback filter is an integrator.

80. (New) The loop of claim 74, wherein the digital feedback filter is a recursive averager.

81. (New) The loop of claim 74, wherein the oversampler is a sigma delta modulator.

82. (New) A method of preprocessing a pulse encoded digital signal for amplification by a digital amplifier, the method including:

oversampling a wide-bit input signal to produce a second signal that has lower bits precision than the input signal;

converting the second signal into a pulse width modulated signal, whereby undesirable distortion is introduced;

digitally filtering the pulse width modulated signal to correct at least part of the undesirable distortion; and

producing a corrected pulse width modulated signal using the correction signal.

83. (New) The method of claim 82, further including:

formatting the correction signal to match bit-width and frequency of the input signal;

feeding back the formatted correction signal and filtering it together with the input signal.

84. (New) The method of claim 83, wherein an integrator is used to filter the formatted correction signal together with the input signal.

85. (New) The method of claim 82, wherein the input signal has about 12 to 24 bits precision per sample.